

**AMENDMENTS TO THE CLAIMS**

Claims 1-89. (Canceled)

90. (Previously presented) A method of forming a CMOS imager comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a first doped region of a second conductivity type in said doped layer, said first doped region being adjacent a field oxide region, said field oxide region being defined by lateral boundaries, a lower surface and an upper surface;

forming a charge storage capacitor such that the entire extent of said charge storage capacitor overlies within said lateral boundaries of said field oxide region and above said upper surface of said field oxide region; and

forming a direct contact between said first doped region and said charge storage capacitor.

Claims 91-92. (Canceled)

93. (Original) The method according to claim 90, wherein said charge storage capacitor is formed by:

forming a first conductive layer over said substrate including said field oxide region;

forming a dielectric layer over said first conductive layer; and

forming a second conductive layer over said dielectric layer.

94. (Original) The method according to claim 93, wherein said first and second conductive layers are independently selected from the group consisting of doped polysilicon, hemispherical grained polysilicon, TiN, poly/WSix, polyTiSi<sub>2</sub>, and poly/WNx/W.

95. (Original) The method according to claim 90, further comprising forming an element of said CMOS imager simultaneously with forming said storage capacitor.

96. (Original) The method according to claim 95, wherein said element is a transistor gate.

97. (Original) The method according to claim 96, further comprising connecting an electrode of said storage capacitor to said transistor gate.

98. (Original) The method according to claim 95, wherein said element is a transfer gate.

99. (Original) The method according to claim 98, further comprising connecting an electrode of said storage capacitor to said transfer gate.

100. (Original) The method according to claim 95, wherein said element is a source follower gate.

101. (Original) The method according to claim 100, further comprising connecting an electrode of said storage capacitor to said source follower gate.

102. (Original) The method according to claim 95, wherein said element is a gate of a global shutter transistor.

103. (Original) The method according to claim 102, further comprising connecting an electrode of said storage capacitor to said gate of said global shutter transistor.

104. (Original) The method according to claim 90, further comprising:

forming a second doped region of said second conductivity type in the doped layer spaced from said first doped region to transfer charge from a charge collection area;

forming a third doped region of said second conductivity type in the doped layer spaced from said second doped region wherein said third doped region effectuates the transfer of charge to a readout circuit; and

forming a fourth doped region of said second conductivity type in the doped layer spaced from said third doped region wherein said fourth doped region is a drain for a reset transistor for said CMOS imager.

105. (Original) The method according to claim 104, wherein said first conductivity type is p-type, and said second conductivity type is n-type.

106. (Original) The method according to claim 104, further comprising forming a photogate over said doped layer between said first and second doped regions.

107. (Original) The method according to claim 106, further comprising connecting an electrode of said storage capacitor to said photogate.

108. (Previously presented) A method of forming a CMOS imager comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a field oxide region within said semiconductor substrate, said field oxide region being defined by lateral boundaries, a lower surface and an upper surface;

forming a first conductive layer over said field oxide region and said substrate;

forming an insulating layer over said first conductive layer;

forming a second conductive layer over said insulating layer;

patterning said first conductive layer, said insulating layer and said second conductive layer to form a storage capacitor and an electrical element of said CMOS imager, wherein the entire extent of said storage capacitor is formed within said lateral boundaries of said field oxide region and over said upper surface of said field oxide region.

109. (Original) The method according to claim 108, further comprising:

forming a first doped region of a second conductivity type in said doped layer and adjacent said field oxide region;

forming a second doped region of said second conductivity type in said doped layer spaced from said first doped region;

forming a third doped region of said second conductivity type in said doped layer spaced from said second doped region and adjacent said electrical element; and

forming a fourth doped region of said second conductivity type in said doped layer spaced from said third doped region.

110. (Original) The method according to claim 109, wherein said first conductivity type is p-type, and said second conductivity type is n-type.

111. (Original) The method according to claim 109, wherein said first doped region, said second doped region, said third doped region and said fourth doped region are doped at a dopant concentration of from about  $1 \times 10^{15}$  ions/cm<sup>2</sup> to about  $1 \times 10^{16}$  ions/cm<sup>2</sup>.

112. (Original) The method according to claim 108, wherein said electrical element is a transistor gate.

113. (Original) The method according to claim 112, further comprising connecting an electrode of said storage capacitor to said transistor gate.

114. (Original) The method according to claim 108, wherein said electrical element is a reset transistor gate.

115. (Original) The method according to claim 114, further comprising connecting an electrode of said storage capacitor to said reset transistor gate.

116. (Original) The method according to claim 108, wherein said electrical element is a source follower transistor gate.

117. (Original) The method according to claim 116, further comprising connecting an electrode of said storage capacitor to said source follower transistor gate.

118. (Original) The method according to claim 108, wherein said electrical element is a row select transistor gate.

119. (Original) The method according to claim 118, further comprising connecting an electrode of said storage capacitor to said row select transistor gate.

120. (Original) The method according to claim 108, wherein said electrical element is a gate of a global shutter transistor.

121. (Original) The method according to claim 120, further comprising connecting an electrode of said storage capacitor to said gate of said global shutter transistor.

122. (Previously presented) A method of forming an imager comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a field oxide region in said semiconductor substrate;

forming a photosensor including a charge collection region of a second conductivity type, said charge collection region being provided in said doped layer, said charge collection region being adjacent one side of a gate of a pixel transistor;

forming a floating diffusion region for receiving charge from said charge collection region, said floating diffusion region being connected to said gate of said pixel transistor and being adjacent another side of said gate opposite said charge collection region; and

forming a charge storage capacitor over said semiconductor substrate so that one electrode of said storage capacitor is connected directly to said floating diffusion region by an electrical contact and the other electrode of said storage capacitor is connected to a gate of another transistor.

123. (Previously presented) The method of claim 122, wherein the entire extent of said charge storage capacitor overlies said field oxide region.

124. (Previously presented) The method of claim 122, wherein the entire extent of said charge storage capacitor overlies an active area of a pixel containing said photosensor.

125. (Previously presented) The method of claim 122, wherein said charge storage capacitor is formed partially over said field oxide region and partially over an active area of a pixel containing said photosensor.

126. (Canceled)

127. (Canceled)

128. (Previously presented) The method of claim 122, wherein said another transistor is part of a three-transistor cell.

129. (Previously presented) The method of claim 122, wherein said another transistor is part of a four-transistor cell.

130. (Previously presented) A method of forming an imager comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a field oxide region in said semiconductor substrate, said field oxide region being defined by lateral boundaries, a lower surface and an upper surface;

forming a photodiode in said doped layer;

forming a charge storage capacitor such that the entire extent of said charge storage capacitor overlies within said lateral boundaries of said field oxide region and over said upper surface of said field oxide region; and

connecting an electrode of a charge storage capacitor directly to said photodiode by an electrical contact.

131. (Previously presented) The method of claim 130, wherein the other electrode of said charge storage capacitor is connected to ground.

132. (Previously presented) The method of claim 130, wherein the other electrode of said charge storage capacitor is connected to a gate of a transistor.

133. (Previously presented) The method of claim 132, wherein said transistor is a transfer transistor.

134. (Previously presented) The method of claim 132, wherein said transistor is a source follower transistor.

135. (Previously presented) The method of claim 132, wherein said transistor is a row select transistor.

136. (Previously presented) The method of claim 135, wherein said transistor is part of a three-transistor cell or of a four-transistor cell.

Claims 137-141. (Canceled)